be achieved if the described techniques are performed in a different order, and/or if components in a described system, architecture, device, or circuit are combined in a different manner, and/or replaced or supplemented by other components or their equivalents. Therefore, the scope of the disclosure is defined not by the detailed description, but by the claims and their equivalents, and all variations within the scope of the claims and their equivalents are to be construed as being included in the disclosure.

What is claimed is:

1. A semiconductor package, comprising:
- a first substrate;
- a pattern layer disposed on the first substrate;
- a first chip member disposed on a surface of the first substrate;
- lead frames disposed on the first substrate surrounding the first chip member; and
- a first encapsulation layer disposed on the first substrate, encapsulating the first chip member and the lead frame,
- wherein upper end portions of the lead frame and the first encapsulation layer are removed, and lead frame columns are exposed through the first encapsulation layer.

2. The semiconductor package of claim **1**, wherein lead frames are provided along four lateral sides of the first chip member.

3. The semiconductor package of claim **1**, further comprising:
- a second substrate disposed on the first encapsulation layer;
- a second chip member disposed on the second substrate; and
- a second encapsulation layer, encapsulating the second substrate and the second chip member.

4. The semiconductor package of claim **3**, wherein the first substrate and the second substrate are connected to each other by a plurality of lead frame columns provided along four sides of the first chip member.

5. The semiconductor package of claim **1**, further comprising:
- a second chip member disposed on another surface of the first substrate, opposite to the surface of the first substrate; and
- a second encapsulation layer, encapsulating the second chip member.

6. The semiconductor package of claim **1**, wherein an upper end portion or a lower end portion, or both end portions, of the lead frame columns comprise a bent part.

7. The semiconductor package of claim **1**, further comprising:
- a solder part disposed on a top surface of the lead frame.

8. The semiconductor package of claim **1**, further comprising:
- mounting electrodes disposed on the surface of the first substrate and another surface of the first substrate.

9. The semiconductor package of claim **8**, wherein the pattern layer electrically connects the mounting electrode on the surface of the first substrate to the mounting electrode disposed on the other surface of the first substrate.

10. A method of manufacturing a semiconductor package, the method comprising:
- preparing a first substrate;
- disposing a first chip member on a surface of the first substrate;
- disposing a lead frame on the surface of the first substrate along a side of the first chip member;
- disposing a first encapsulation layer onto the surface of the first substrate, wherein the first encapsulating layer encapsulates the first chip member and the lead frame; and
- removing upper end portions of the first encapsulation layer and the lead frame.

11. The method of claim **10**, wherein lead frames are connected to each other by a support.

12. The method of claim **11**, wherein the support is removed together with the upper end portion of the lead frame.

13. The method of claim **10**, wherein upper end portions of the first encapsulation layer and the lead frame are removed by polishing, grinding, or cutting.

14. The method of claim **10**, wherein an upper end portion, or a lower end portion, or both end portions of the lead frame comprise a bent part.

15. The method of claim **10**, further comprising, after the removing of the upper end portions of the first encapsulation layer and the lead frame,
- disposing a second substrate on the first encapsulation layer and the lead frame;
- disposing a second chip member on the second substrate; and
- disposing a second encapsulation layer, encapsulating the second chip member.

16. The method of claim **10**, further comprising:
- after the removing of the upper end portions of the first encapsulation layer and the lead frame,
- disposing a second chip member onto another surface of the first substrate; and
- disposing a second encapsulation layer, encapsulating the second chip members.

17. The method of claim **10**, wherein the lead frame is provided to form a plurality of columns adjacent to each lateral side of the first chip member.

18. The method of claim **10**, further comprising:
- after the removing of the upper end portions of the first encapsulation layer and the lead frame:
- disposing a solder part on the lead frame.

19. The method of claim **10**, further comprising:
- disposing mounting electrodes on the surface of the first substrate and another surface of the first substrate.

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